CLAIMS

What is claimed is:

1. A semiconductor package having conductive bumps on a chip, comprising:

at least one chip having an active surface and an opposite inactive surface, and having a plurality of bond pads formed on the active surface;

a plurality of conductive bumps respectively formed on the bond pads of the chip;

an encapsulation body for encapsulating the chip and the conductive bumps, wherein ends of the conductive bumps are exposed outside of the encapsulation body and flush with a surface of the encapsulation body;

a plurality of first conductive traces formed on the surface of the encapsulation body and electrically connected to the exposed ends of the conductive bumps;

a solder mask layer applied over the first conductive traces and having a plurality of openings for exposing predetermined portions of the first conductive traces; and

a plurality of solder balls respectively formed on the exposed portions of the first conductive traces.

2. The semiconductor package of claim 1, further comprising: at least one dielectric layer and a plurality of second conductive traces formed on the dielectric layer, the dielectric layer and the second conductive traces interposed between the first conductive traces and the solder mask layer, wherein the dielectric layer is located on the first conductive traces and has a plurality of vias by which the predetermined portions of the first conductive traces are exposed and electrically connected to the second conductive traces, and the solder mask layer is located on the second conductive traces whose predetermined portions are exposed via the openings of the solder mask layer and respectively connected to the plurality of solder balls.

3. The semiconductor package of claim 1, wherein the inactive surface of the chip is exposed outside of the encapsulation body.
4. The semiconductor package of claim 2, wherein the inactive surface of the chip is exposed outside of the encapsulation body.
5. The semiconductor package of claim 1, wherein the conductive bump is selected from the group consisting of solder bump, high lead solder bump, gold bump, and gold stud bump.
6. The semiconductor package of claim 2 wherein the conductive bump is selected from the group consisting of solder bump, high lead solder bump, gold bump, and gold stud bump.
7. The semiconductor package of claim 1, wherein the exposed portions of the first conductive traces are terminals.
8. The semiconductor package of claim 2, wherein the exposed portions of the second conductive traces are terminals.
9. A method for fabricating a semiconductor package having conductive bumps on a chip, comprising the steps of:

preparing a wafer comprising a plurality of chips, each chip having an active surface and an opposite inactive surface, and having a plurality of bond pads formed on the active surface;

forming a plurality of conductive bumps respectively on the bond pads of each of the chips;

singulating the wafer to separate the plurality of chips, each chip having a plurality of the conductive bumps thereon;

providing a carrier for accommodating the plurality of chips, and mounting the conductive bumps of each of the chips on a surface of the carrier;

forming an encapsulation body on the surface of the carrier for encapsulating the

chips and the conductive bumps;

removing the carrier to allow ends of the conductive bumps to be exposed outside of the encapsulation body and flush with a surface of the encapsulation body;

forming a plurality of conductive traces on the surface of the encapsulation body and electrically connecting the conductive traces to the exposed ends of the conductive bumps;

applying a solder mask layer over the conductive traces and forming a plurality of openings through the solder mask layer for exposing predetermined portions of the conductive traces;

depositing a plurality of solder balls respectively on the exposed portions of the conductive traces; and

cutting the encapsulation body to form a plurality of individual semiconductor packages each having at least one of the singulated chips.

10. The method of claim 9, further comprising a step of: prior to forming the plurality of conductive traces, performing a grinding process to grind the surface of the encapsulation body flush with the ends of the conductive bumps.
11. The method of claim 9, further comprising a step of: prior to forming the plurality of conductive traces, performing a grinding process to grind the surface of the encapsulation body flush with the ends of the conductive bumps, and grind off a portion of the encapsulation body covering the inactive surfaces of the chips to expose the inactive surfaces.
12. The method of claim 9, wherein the conductive bump is selected from the group consisting of solder bump, high lead solder bump, gold bump, and gold stud bump.
13. The method of claim 9, wherein the exposed portions of the conductive traces are terminals.

14. The method of claim 9, wherein the carrier is a tape.

15. A method for fabricating a semiconductor package having conductive bumps on a chip, comprising the steps of:

preparing a wafer comprising a plurality of chips, each chip having an active surface and an opposite inactive surface, and having a plurality of bond pads formed on the active surface;

forming a plurality of conductive bumps respectively on the bond pads of each of the chips;

singulating the wafer to separate the plurality of chips, each chip having a plurality of the conductive bumps thereon;

providing a carrier for accommodating the plurality of chips, and mounting the conductive bumps of each of the chips on a surface of the carrier;

forming an encapsulation body on the surface of the carrier for encapsulating the chips and the conductive bumps;

removing the carrier to allow ends of the conductive bumps to be exposed outside of the encapsulation body and flush with a surface of the encapsulation body;

forming a plurality of first conductive traces on the surface of the encapsulation body and electrically connecting the first conductive traces to the exposed ends of the conductive bumps;

coating at least one dielectric layer on the first conductive traces and forming a plurality of vias through the dielectric layer for exposing predetermined portions of the first conductive traces;

forming a plurality of second conductive traces on the dielectric layer and electrically connecting the second conductive traces to the exposed portions of the first conductive traces;

applying a solder mask layer over the second conductive traces and forming a

plurality of openings through the solder mask layer for exposing predetermined portions of the second conductive traces;

depositing a plurality of solder balls respectively on the exposed portions of the second conductive traces; and

cutting the encapsulation body to form a plurality of individual semiconductor packages each having at least one of the singulated chips.

16. The method of claim 15, further comprising a step of: prior to forming the first conductive traces, performing a grinding process to grind the surface of the encapsulation body flush with the ends of the conductive bumps.

17. The method of claim 15, further comprising a step of: prior to forming the first conductive traces, performing a grinding process to grind the surface of the encapsulation body flush with the ends of the conductive bumps, and grind off a portion of the encapsulation body covering the inactive surfaces of the chips to expose the inactive surfaces.

18. The method of claim 15, wherein the conductive bump is selected from the group consisting of solder bump, high lead solder bump, gold bump, and gold stud bump.

19. The method of claim 15, wherein the exposed portions of the second conductive traces are terminals.

20. The method of claim 15, wherein the carrier is a tape.